In the drawings:

In Fig. 1 delete reference numeral 16.

In Fig. 2, change reference numeral "102" to - - 119 - -; change reference numeral "100" to - - 130 - -; change reference numeral "88" to - - 186 - -; reverse reference numerals "22" and "26"; reverse reference numerals "11" and "13"; change reference numeral "86" to - - 86' - -; change reference numeral "76" to - - 76' - -; and delete reference numeral 29 and the arrow.

In the specification:

Please amend the section of the specification labeled "Detailed Description of the Invention," as indicated below. Underlined text indicates new text while struckthrough or bracketed text indicates deleted text.

Please replace paragraph beginning at page 5, ln. 25 to page 6, ln. 7 as follows:

A column-wise adjacent cell 115 has the same components as cell 15, namely an MOS transistor 135 connected as a plate capacitor, a current injector formed by a diode 129 and injector transistor 121, an EEPROM memory transistor 123 and a capacitive device 125. A current meter 139 reads the output of memory transistor 123 along bit line 137. Programming lines 11 and 13 bias the current injector for conduction when appropriate bias is established by actuation line 133, with electrons driven to the floating gate of memory transistor 123. The method of charge injection into the oxide and floating gate or from the floating gate into the oxide and substrate can be any of the following mechanisms: photo-emission, Fowler-Nordheim tunneling, hot electron injection at appropriate temperatures (i.e. not lower than 500°C), or Zener or Avalanche breakdown (i.e. if carriers in substrate acquire energies in excess of the electron or hole barrier height). Other cells in the memory array, such as cells 215 and 315 have similar components as memory cells 15 and 115, respectively.

Please replace paragraph beginning at page 6, ln. 28 to page 7, ln. 35 as follows:

In the memory cell 15 of Fig. 2, two programming lines 11 and 13 control operation of injector transistor ~~31~~ 21 that can reverse bias diode 29. Recalling that this reverse bias of diode 29 generates impact ionization current that stores charge in the floating gate of memory transistor 23. But memory transistor 23 was said to have a device 25 in a capacitive relation with respect to word line 19. The device 25 has a polysilicon plate 30 having a first finger or tang [[86]] 86' that serves as control gate of memory transistor 23 actuated by word line 19. The word line 19 may be over or under plate 25, separated by an insulative layer, such as oxide. In the case of being under plate 25, the word line 19 may be a buried word line in an n-well diffusion in order to save space. Another tang [[88]] 186 extends out of memory cell 15 to an adjacent injector transistor as a control gate for the injector. Voltage on the word line 19 is capacitively coupled to plate 30 thereby providing voltage for erasing EEPROM memory transistor 23. Simultaneously, the plate provides a voltage to a control gate of an injector transistor in an adjacent cell. In other words, each injector transistor has a control gate that is a tang of a polysilicon plate, such as plate 30. In the case of injector transistor 21, tang [[90]] 76' projecting from polysilicon plate [[100]] 130 provides voltage via capacitive coupling with word line [[102]] 119. Recall that voltage bias on line 33 charges line 36, stimulating impact ionization from diode 29 that passes through a common substrate toward memory transistor 23. Since line 36 serves as floating gate for the memory transistor, the floating gate remains charged, even after bias is removed from line 31. The role of tang [[90]] 76' is to augment voltage applied to the control gate of transistor 21 and to allow word line control of programming. In the latter mode of operation,

an entire row (or column) of memory cells could be programmed or erased under word line control. In the former mode of operation, some of the voltage for programming or erasing is coupled through a word line, but another part of the needed voltage is supplied by a voltage applied on line 33, thereby allowing programming and erase control of individual cells. The circuit topology of Fig. 2 is closer to an actual layout of a cell, compared to Fig. 1, because word lines are at right angles to bit lines.

Please replace section beginning at page 8, ln. 20 to page 10, ln. 7 as follows:

The following is the correspondence between elements of Figs. 1 and 2 and features shown in Fig. 3. Vias 72 and 74 of Fig. 3 terminate in contacts 22 and 26 of Figs. 1 and 2. Diode 29 of Figs. 1 and 2 is formed p-n junction 62 and 81 of Fig. 3. Subsurface N region 62 is connected by via 72 in Fig. 3 to program line 11 at contact 22 in Figs. 1 and 2. Subsurface p region 64 is connected by via 74 in Fig. 3 to bit line 13 at contact 26 in Figs. 1 and 2. Subsurface region 91 contacted by via 90 is the actuation line 33 for bias of the first memory cell 15 in Fig. 1. Control poly ~~Poly~~ gate 76 is joined to control poly gate 86 by a line, represented by line 85 in Fig. 3 and the connected gates of transistors 21 and 23 in Figs. 1 and 2. Control poly ~~Poly~~ gate 76 is tang [[90]] 76' of poly plate [[100]] 130 in Fig. 2 that may be controlled by voltages applied to word line [[102]] 119. The same gate is also controlled by voltage applied on line 33 of MOS device 35 for biasing of the gate to establish writing or programming in transistor 23. With word line control, a block of memory transistors may be programmed at the same time. With gate control from device 33, a single transistor is programmed.

In Fig. 3, the via 97 communicates with current meter 39, seen in Figs. 1 and 2, through contact 32. Memory

transistor 23 has a control poly gate 86 spaced between source 82 and drain 84, in turn communicating through vias 97 and 99 to the source 82 and the drain 84 ~~contacts 28 and 32, respectively, seen in Figs. 1 and 2~~. Subsurface region 93 connected by via 94 for external contact is actuation line 133 for bias of the second memory cell 115 in Fig. 1. Recall that transistor 23 has a floating gate formed three gate leads for transistors 35, 21, and 22 seen in Figs. 1 and 2. The gate leads are represented by dashed line 85 in Fig. 3. Control gate 86 is a tang [[86]] 86' of poly plate 30 of device [[25]] 23 seen in Fig. 2. Contact 32 is associated with current meter 39 on line 37. Each well may have a current meter although only the current meter 39 associated with measuring charge on a memory cell is discussed herein.

In Fig. 3, the transistor 223 is a memory transistor of an adjacent cell. The transistor 223 is symmetric with transistor 23 having a shared electrode 84 and source electrode 88. The via 99 above shared electrode 84 forms a plane of symmetry except for current measuring electrodes and provides bias for associated transistors 23 and 223, similar to via 90 and subsurface region 91, but using actuation line 201 seen in Fig. 4. Control poly region 92 is a tang of another poly plate and so is poly region 176 of injection transistor 221. The floating gate for memory transistor 223 is actually formed by three gate leads, analogous to the leads of transistors 35, 21, and 23, indicated by dashed line 185. To the right of p-well 65 is p-well 67, separated by isolation region 77. The doped n-implants 162 and 164 are in p-well 67, below conductive vias 172 and 174. The implants 162 and 164 define electrodes for MOS injection transistor 221. A cooperating part of the current injector is formed by a diode having p-implanted region 181 abutting n+ region 162. The diode is made by implants at the same time and in the same manner as the diode associated with transistor 21. The diode is controlled by transistor 221, having control gate 176,

operating in the same manner as transistor 21. Electrons for charge storage on floating gates 85 and 185 are generated by this impact ionization. These electrons are involved in transfer to the floating gates by tunneling hot electron injection or other known mechanisms.

Please replace paragraph beginning at page 10, ln. 13 to page 10, ln. 36 as follows:

One of the remarkable features of the present invention is illustrated in Fig. 4. The word line 19 is seen to lie under or over poly plate 30. The poly plate 30 has a pair of tangs [[86]] 86' and 186, extending in opposite directions. The tang [[86]] 86' is the control gate 86 of memory transistor 23. See Fig. 3. The tang 186 is the control gate of an injector transistor in another row. Voltage on word line 19 induces voltage on poly plate 30, a capacitor-like device. Tang [[86]] 86' causes erasing of memory cell 23 while tang 186 initiates impact ionization current in an injector transistor in another row and hence writing in another row. This is similar to action by poly plate 130, spaced over or under word line 119 by an insulative layer, such as oxide, and having tang 76 projecting into injector transistor 21 as its control gate. Voltage on word line 119 induces voltage on poly plate 130 and hence on tang 76. This voltage initiates impact ionization current that stores charge in the floating gate of memory transistor 23. Shared line 101, a common electrode for memory transistor 23 and 223 in Fig. 3, is an axis of symmetry for structures to the right, except for current measuring lines. Lateral symmetry allows two memory transistors to share the same well and achieve a good degree of compactness.